Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. -39. (Cancelled)

40~~62~~. (currently amended) A method comprising:

a) driving a first current through a line and a termination resistance so that a logical value on said line changes from a first logical value to a second logical value, said first current sustained for a width of a first bit that is propagated on said line; and,

b) holding said second logical value on said line by driving a second current through said line and said termination resistance, said second current less than said first current, said second current sustained for a width of a second bit that is propagated on said line.

41~~63~~. (currently amended) The method of claim 40~~62~~ wherein said first and second currents flow in a direction from said line into said termination resistance.

42~~64~~. (currently amended) The method of claim 41~~63~~ wherein said second logical value is a logical high.

4365. (currently amended) The method of claim 4163 wherein said first current produces a first voltage on said line that is larger than a second voltage produced on said line by said second current.

4466. (currently amended) The method of claim 4062 wherein said first and second currents flow in a direction from said termination resistance into said line.

4567. (currently amended) The method of claim 4466 wherein said second logical value is a logical low.

4668. (currently amended) The method of claim 4466 wherein said first current produces a first voltage on said line that is smaller than a second voltage produced on said line by said second current.

4769. (currently amended) The method of claim 4062 wherein said first bit width is coextensive with a clock cycle.

4870. (currently amended) The method of claim 4062 wherein said driving a first current further comprises applying a first multiplexer select line state to a multiplexer so that a first word is provided at an output of said multiplexer, said first word enabling a first number of sub-drivers, and said driving a second current further comprises applying a second multiplexer select line state to said multiplexer so that a second word is provided at said output of said multiplexer, said second word

enabling a second number of said sub-drivers, said first number greater than said second number.

4971. (currently amended) An apparatus, comprising:

a driver that drives a line that is terminated with a termination resistance, said termination resistance coupled to a termination voltage, said driver designed to drive said line to a first voltage if a logical value on said line needs to be changed from a first logic level to a second logic level, said driver designed to drive said line to a second voltage if said second logic level on said line does not need to be changed, the squared difference between said first voltage and said termination voltage being greater than the squared difference between said second voltage and said termination voltage, said first and second voltages each capable of being interpreted as said second logic level.

5072. (currently amended) The apparatus of claim 4971 wherein said first voltage is reached during a first bit width and said second voltage is reached during a second, following bit width.

5173. (currently amended) The apparatus of claim 4971 wherein said driver further comprises a plurality of sub-drivers, each of said sub-drivers designed to drive said line, a first number of said sub-drivers designed to drive said line to said first voltage, a second number of said sub-drivers designed to drive said line to said second voltage, said first number larger than said second number.

52~~74~~. (currently amended) The apparatus of claim 51~~73~~ wherein said first number corresponds to all of said sub-drivers.

53~~75~~. (currently amended) The apparatus of claim 51~~73~~ further comprising a multiplexer that alternatively issues a first word and a second word, said first word to enable said first number of said sub-drivers, said second word to enable said second number of said sub-drivers.

54~~76~~. (currently amended) The apparatus of claim 49~~71~~ wherein said line is an address line that addresses a memory device.

55~~77~~. (currently amended) The apparatus of claim 54~~76~~ wherein said second voltage appears on said line during the later cycles of a burst read from said memory.

56~~78~~. (currently amended) The apparatus of claim 55~~77~~ wherein said memory is a DDR-SDRAM memory device.

57~~79~~. (currently amended) A method, comprising:

a) driving a line to a first voltage if said line's logic level needs to be changed from a first logic level to a second logic level, said line terminated with a termination resistance, said termination resistance coupled to a termination voltage; and,

b) driving said line to a second voltage if said line's logic level does not need to be changed back to said first logic level after having been said changed from said first logic level to said second logic level, said first and second voltages capable of being interpreted as said second logic level, the squared difference of said first voltage and said termination voltage being greater than the squared difference of said second voltage and said termination voltage.

5880. (currently amended) The method of claim 5779 wherein said first voltage is reached during a first bit width and said second voltage is reached during a second, following bit width.

5981. (currently amended) The method of claim 5779 wherein said driving said line to said first voltage further comprises enabling a first number of sub-drivers, said driving said line to said second voltage further comprises enabling a second number of said sub-drivers, said first number larger than said second number.

6082. (currently amended) The method of claim 5779 further comprising issuing a first word from a multiplexer in order to said enable said first number of sub-drivers and issuing a second word from a multiplexer in order to said enable said second number of said sub-drivers.

6183. (currently amended) The method of claim 5779 wherein said line is an address line that addresses a memory device.

62~~84~~. (currently amended) The method of claim 61~~83~~ wherein said second voltage appears on said line during the later cycles of a burst read from said memory.

63~~85~~. (currently amended) The method of claim 62~~84~~ wherein said memory is a DDR-SDRAM memory device.

64~~86~~. (currently amended) An apparatus, comprising:

a) means for driving a line to a first voltage if said line's logic level needs to be changed from a first logic level to a second logic level, said line terminated with a termination resistance, said termination resistance coupled to a termination voltage; and,

b) means for driving said line to a second voltage if said line's logic level does not need to be changed back to said first logic level after having been said changed from said first logic level to said second logic level, said first and second voltages capable of being interpreted as said first logic level, the squared difference of said first voltage and said termination voltage being greater than the squared difference of said second voltage and said termination voltage.

65~~87~~. (currently amended) The apparatus of claim 64~~86~~ wherein said first voltage is reached during a first bit width and said second voltage is reached during a second, following bit width.

6688. (currently amended) The apparatus of claim 6486 further comprising means for driving said line to said first voltage with a first number of sub-drivers, and comprising means for said driving said line to said second voltage with a second number of sub-drivers, said first number larger than said second number.

6789. (currently amended) The apparatus of claim 6688 further comprising means for issuing a first word in order to said enable said first number of sub-drivers and issuing a second word in order to said enable said second number of sub-drivers.

6890. (currently amended) The apparatus of claim 6486 wherein said line is an address line that addresses a memory device.

6991. (currently amended) The apparatus of claim 6890 wherein said second voltage appears on said line during the later cycles of a burst read from said memory.

7092. (currently amended) The apparatus of claim 6890 wherein said memory is a DDR-SDRAM memory device.

71. (new) An apparatus to drive a logic level with multiple current strengths, comprising:

a plurality of drivers each having a enable/disable input, each said enable/disable input coupled to an output of a multiplxer, said mutliplexer having a

first group of inputs and a second group of inputs, said first group of multiplexer inputs to provide an indication of a first number of said drivers to be enabled while driving a logic level with a first current strength, said second group of multiplexer inputs to provide an indication of a second number of said drivers to be enabled while driving a logic level with a second current strength.

72. (new) The apparatus of claim 71 wherein said first number is greater than said second number and said first current strength is greater than said second current strength.

73. (new) The apparatus of claim 71 wherein said first group of multiplexer inputs are coupled to a group of register outputs.

74. (new) The apparatus of claim 71 wherein said multiplexer's channel select input is coupled to a signal line, said signal line to carry a signal that indicates when said logic level is to be driven with said first current strength and when said logic level is to be driven with said second current strength.

75. (new) The apparatus of claim 72 wherein each driver of said plurality of drivers also has a second enable/disable input, each of said enable/disable inputs to enable/disable a P channel transistor within its respective driver, said P channel transistor to push current over a line, each of said second enable/disable inputs to enable/disable an N channel transistor within its respective driver, said N channel

transistor to pull current from said line, said second enable/disable inputs coupled to an output of a second multiplexer.

76. (new) The apparatus of claim 75 wherein said second mutliplexer has a first group of inputs and a second group of inputs, said first group of multiplexer inputs to provide an indication of a first number of said drivers to have an enabled P channel transistor while driving said logic level with a first current strength, said second group of multiplexer inputs to provide an indication of a second number of said drivers to have an enabled P channel transistor while driving a logic level with a second current strength, said first group of second multiplexer inputs to provide an indication of a first number of said drivers to have an enabled N channel transistor while driving said logic level with a first current strength, said second group of second multiplexer inputs to provide an indication of a second number of said drivers to have an enabled N channel transistor while driving a logic level with a second current strength.

77. (new) The apparatus of claim 76 wherein said first group of first multiplexer inputs are coupled to a first group of first register outputs and said first group of second multiplexer inputs are coupled to a second group of register outputs.

78. (new) The apparatus of claim 76 wherein a first channel select input of said first multiplexer and a second channel select input of said second multiplexer are both coupled to a signal line, said signal line to carry a signal that indicates when said

logic level is to be driven with said first current strength and when said logic level is to be driven with said second current strength.

79. (new) An apparatus, comprising:

a DDR memory comprising address lines that are coupled to a plurality of drivers, each of said drivers having an enable/disable input, each said enable/disable input coupled to an output of a multiplexer, said mutliplexer having a first group of inputs and a second group of inputs, said first group of multiplexer inputs to provide an indication of a first number of said drivers to be enabled while driving a logic level with a first current strength, said second group of multiplexer inputs to provide an indication of a second number of said drivers to be enabled while driving a logic level with a second current strength.

80. (new) The apparatus of claim 79 wherein said first number is greater than said second number and said first current strength is greater than said second current strength.

81. (new) The apparatus of claim 79 wherein said first group of multiplexer inputs are coupled to a group of register outputs.

82. (new) The apparatus of claim 79 wherein said multiplexer's channel select input is coupled to a signal line, said signal line to carry a signal that indicates when said

logic level is to be driven with said first current strength and when said logic level is to be driven with said second current strength.

83. (new) The apparatus of claim 80 wherein each driver of said plurality of drivers also has a second enable/disable input, each of said enable/disable inputs to enable/disable a P channel transistor within its respective driver, said P channel transistor to push current over a line, each of said second enable/disable inputs to enable/disable an N channel transistor within its respective driver, said N channel transistor to pull current from said line, said second enable/disable inputs coupled to an output of a second multiplexer.

84. (new) The apparatus of claim 83 wherein said second mutliplexer has a first group of inputs and a second group of inputs, said first group of multiplexer inputs to provide an indication of a first number of said drivers to have an enabled P channel transistor while driving said logic level with a first current strength, said second group of multiplexer inputs to provide an indication of a second number of said drivers to have an enabled P channel transistor while driving a logic level with a second current strength, said first group of second multiplexer inputs to provide an indication of a first number of said drivers to have an enabled N channel transistor while driving said logic level with a first current strength, said second group of second multiplexer inputs to provide an indication of a second number of said drivers to have an enabled N channel transistor while driving a logic level with a second current strength.

85. (new) The apparatus of claim 84 wherein said first group of first multiplexer inputs are coupled to a first group of first register outputs and said first group of second multiplexer inputs are coupled to a second group of register outputs.

86. (new) The apparatus of claim 84 wherein a first channel select input of said first multiplexer and a second channel select input of said second multiplexer are both coupled to a signal line, said signal line to carry a signal that indicates when said logic level is to be driven with said first current strength and when said logic level is to be driven with said second current strength.

COMMENTS

The enclosed is responsive to the Examiner's Office Action mailed on October 25, 2004. According to the Examiner's Office Action mailed 10/25/04, claims 1-39 were pending. However, the Applicants filed a preliminary amendment on August 18, 2003 in which claims 1-39 were canceled. As such, the Examiner has provided a response to claims that were intended to be canceled.

After a phone conversation held with the Examiner on January 13, 2005, the Examiner indicated that the Examiner's outstanding Office Action mailed on 10/25/05 should be responded to by the Applicants with the correct listing of claims; and that, the Examiner will essentially generate a new response. According to the Examiner, the present response will not be considered by the Examiner when deciding if a first Final Office Action is merited in the present application.

The Applicants have included herewith a proper listing of all claims to be considered in the present application that regards the aforementioned preliminary amendment as having been filed on 8/18/03. Because the Applicants' preliminary amendment incorrectly numbered the claims, the present response includes amendments to the claims numbers to cure the defects in the 8/18/03 preliminary amendment. Moreover, new claims 71 – 86 that are to be added to those claims entered by way of the 8/18/03 preliminary amendment have been added by way of the present response.

Because the Examiner's Office Action was directed to the incorrect set of claims, the Applicant refrains from providing any substantive comments in response

to the Examiner's 10/25/04 Office Action. Applicant notes, however, that the Examiner's allowance of independent claim 11 in the Examiner's 10/25/04 Office Action should correspond to an allowance of independent claim 62.

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact Robert B. O'Rourke at (408) 720-8300.

Respectfully submitted,

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